



# High Performance Embedded Computing Workshop

23 – 25 September 2008

## AGENDA

23 – 25 September

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### Workshop at a Glance

**Day 1**  
23 September

Check-in / Setup: 0730  
Welcome: 0830

**Keynote Address**

**Opening Remarks**

Sessions: **Session 1:** New Application Frontiers

**Poster / Demo A:** Advanced Systems

**Session 2:** Multicore Architecture

**Focus 2:** Multicore Applications

*(Session 2 and Focus 2 run in parallel)*

Adjourn: 1700

1745 **Reception**

1845 **Banquet Speaker**

1930 **Banquet**

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**Day 2**  
24 September

Check-in / Setup: 0730  
Announcements: 0830

**Keynote Address**

Sessions: **Session 3:** GPUs

**Focus 3:** FPGA

*(Session 3 and Focus 3 run in parallel)*

**Poster / Demo B:** Novel Computing Hardware

**Session 4:** Networking

**Focus 4:** Cell

*(Session 4 and Focus 4 run in parallel)*

**Panel:** Paving the Way for Multicore Open Systems Architectures

Adjourn: 1715

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**Day 3**  
25 September

Check-in / Setup: 0730  
Announcements: 0830

Sessions: **Session 5:** Innovative Software Tools

**Focus 5:** Benchmarking

*(Session 5 and Focus 5 run in parallel)*

**Poster / Demo C:** Multicore Programming Environments

**Session 6:** Awards Session

Adjourn: 1700

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### 23 September

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- 0730 **Check-in / Poster Setup / Continental Breakfast**
- 0830 **Welcome**  
Mr. David Martinez / MIT Lincoln Laboratory
- 0835 **Mission Keynote Speaker:**  
Mr. Randy Walden / Air Force Rapid Capabilities Office (SAF/RCO)
- 0920 **Opening Remarks**  
Mr. Robert Bond / MIT Lincoln Laboratory
- 0925 **Invited: Case Studies Optimizing Applications for a 50 TFLOPS Cluster of PS3s**  
Richard Linderman / AFRL
- 0955 

<b>Session 1: New Application Frontiers</b> Chair: Kenneth Teitelbaum / MIT Lincoln Laboratory <b>Auditorium</b>
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- 1005 **Invited: New Sensor Signal Processing Paradigms: When One Pass Isn't Enough**  
Ed Baranoski / Argon ST
- 1035 **Break**
- 1050 **Invited: Plug-and-Play Approaches for the Creation of Rapid Space Systems**  
James Lyke / AFRL RV
- 1120 **Linear Algebraic Graph Algorithms for Back End Processing**  
*Jeremy Kepner*, Nadya Bliss and Eric Robinson / MIT Lincoln Laboratory

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### 23 September (Continued)

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1150

**Poster / Demo A: Advanced Systems**

Chair: Kenneth Teitelbaum / MIT Lincoln Laboratory

1200 **Poster / Demo A Précis**

- Poster A.1** **Multicore Acceleration of the Complex Ambiguity Function**  
*Douglas Enright*, Eric Dashofy, Michael AuYeung, R. Scott Boughton, J. Matt Clark and Ronald Scrofano, Jr. / The Aerospace Corporation
- Poster A.2** **Re-Mapping of a Reconfigurable Generic Search DSP (RGSD) and a Generic Air Track Processor (GATP) to Multicore Technology with Linux SMP**  
*Robert Hamilton* and Bernard Pelon / CSP, Inc.  
Steve Shank, John Johansson, Rick Pancoast and Leon Trevito / Lockheed Martin MS2
- Poster A.3** **Efficient Multidimensional Polynomial Filtering for Nonlinear Digital Predistortion**  
*Matthew Herman*, Benjamin Miller and Joel Goodman / MIT Lincoln Laboratory
- Poster A.4** **Designing Processing Architectures for Space Applications**  
*John Holland* and Eliot Glaser / Northrop Grumman Corporation
- Poster A.5** **2D-3D Registration of Optical and Ladar Imagery for Real-Time Tracking**  
*Andrew Mastin* / MIT Lincoln Laboratory, Massachusetts Institute of Technology  
Jeremy Kepner / MIT Lincoln Laboratory  
John Fisher III / Massachusetts Institute of Technology
- Poster A.6** **Leveraging Multi-Core Processors in a CDMA-2000 SDR Base Station**  
*Steve Muir*, John Chapin, Andrew Chiu, Victor Lum and Jeremy Nimmer / Vanu, Inc.
- Poster A.7** **Channelization and Resampling Using a Graphics Processing Unit**  
Ambrose Slone, *Paul Otto* and Aqsa Kuraishi / SAIC
- Poster A.8** **Multi-Processor Defense Applications Implemented Utilizing the Message Distribution Framework (MDF)**  
Philip Barile, Joseph Cook and *Edward Kosinski* / Lockheed Martin MS2
- Poster A.9** **High Performance Processing with MONARCH - A Case Study in CT Reconstruction**  
*Kenneth Prager* / Raytheon Company  
David Rohler / Multi-Dimensional Imaging  
Pat Marek and Lloyd Lewins / Raytheon Company
- Poster A.10** **Embedded Computing Architecture for High Frequency Wideband Sonar Systems**  
*Alan Davis* and Sudha Reese / Naval Undersea Warfare Center
- Poster A.11** **Optimization of Embedded Linux Systems without FPU**  
Sergey Panasyuk / SUNY Institute of Technology  
*Scott Spetka* / SUNY Institute of Technology, ITT Corp.
- Poster A.12** **Radar Pulse Compression Using the NVidia CUDA Framework**  
*Stephen Bash*, David Carpman and David Holl / MIT Lincoln Laboratory
- 1235 **Lunch** (View Posters)

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### 23 September (Continued)

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|------|---|------|--|
| 1330 | <b>Session 2: Multicore Architecture</b><br>Chair: Martin Herbordt / Boston University<br><b>Auditorium</b>   | 1330 | <b>Focus 2: Multicore Applications</b><br>Chair: Larry Bergman / Jet Propulsion Laboratory<br><b>Room S2-180</b>   |
| 1340 | <b>Experience and Results Porting HPEC Benchmarks to MONARCH</b><br><i>Lloyd Lewins</i> and Kenneth Prager / Raytheon Company   | 1340 | <b>High-Performance, Parallel Embedded Architectures Using Acalis® CPU872 PowerPC® Multicore</b><br><i>John Swensen</i> and Gail Walters / CPU Technology Inc.   |
| 1410 | <b>Building Manycore Processor-to-DRAM Networks Using Monolithic Silicon Photonics</b><br><i>Ajay Joshi</i> , Christopher Batten and Vladimir Stojanović / Massachusetts Institute of Technology<br>Krste Asanović / University of California at Berkeley   | 1410 | <b>Porting Some Key Caltech &amp; JPL Applications to a PS3 Cluster - A Wild Ride</b><br><i>Ed Upchurch</i> / Caltech, Jet Propulsion Laboratory<br>Paul Springer / Jet Propulsion Laboratory<br>Mark Stalzer, Sean Mauch, John McCorquodale, and Jan Lindheim / Caltech |
| 1440 | <b>Photonic Many-Core Architecture Study</b><br><i>Nadya Bliss</i> / MIT Lincoln Laboratory<br>Krste Asanović / University of California at Berkeley<br>Keren Bergman and Luca Carloni / Columbia University<br>Jeremy Kepner / MIT Lincoln Laboratory<br>Vladimir Stojanović / Massachusetts Institute of Technology | 1440 | <b>Introspection-Based Fault Tolerance for Future On-Board Computing Systems</b><br>Mark James and <i>Hans Zima</i> / Jet Propulsion Laboratory, California Institute of Technology  |
| 1510 | <b>Break</b> (View Posters)   |      | <b>Transition to the Auditorium</b>  |
| 1525 | <b>When Multicore Isn't Enough: Trends and the Future for Multi-Multicore Systems</b><br><i>Matthew Reilly</i> / SiCortex, Inc.   |      |  |
| 1555 | <b>Invited: Cloud-in-the-Can: Macro-architectures and Programming Models</b><br>Bill Butera / Mitsubishi Electric Research Laboratories   |      |  |
| 1625 | <b>Closing Remarks / Adjourn</b><br>Jeremy Kepner / MIT Lincoln Laboratory  |      |  |
| 1745 | <b>Reception &amp; 2007 Awards</b>  |      |  |
| 1845 | <b>Banquet Speaker:</b><br>Dr. Richard Stallman / Free Software Foundation  |      |  |
| 1930 | <b>Banquet</b>  |      |  |

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0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Announcements**

Mr. Robert Bond / MIT Lincoln Laboratory

0835 **Technology Keynote Speaker:**

Dr. Charles Morefield / DARPA IPTO

0920 **Session 3: GPUs**

Chair: Peter Boettcher / MIT Lincoln Laboratory  
Auditorium

0930 **Using GPUs to Enable Highly Reliable Embedded Storage**

*Matthew Curry* and Anthony Skjellum / University of Alabama

H. Lee Ward and Ron Brightwell / Sandia National Laboratories

1000 **Extending VForce to Include Support for NVIDIA GPUs Using CUDA**

Dennis Cuccaro, *Nicholas Moore* and Miriam Leaser / Northeastern University

Laurie Smith King / College of the Holy Cross

1030 **Break**

1045 **GPU VSIPL: High-Performance VSIPL Implementation for GPUs**

Andrew Kerr, *Dan Campbell* and Mark Richards / Georgia Institute of Technology

1115 **Power Consumption of Desktop and Mobile GPU's for IRSTAP Applications**

*Michael Roeder*, Jeremy Furtek, Nolan Davis, Cezario Tebcherani, Masatoshi Tanida and Dennis Braunreiter / SAIC

0920 **Focus 3: FPGA**

Chair: Michael Vai / MIT Lincoln Laboratory  
Room S2-180

0930 **2D Phase Unwrapping on FPGAs and GPUs**

*Sherman Braganza* and Miriam Leaser / Northeastern University

1000 **Multicore Versus FPGA in the Acceleration of Discrete Molecular Dynamics**

Tony Dean, Josh Model and

*Martin Herbordt* / Boston University

1030 **An Ethernet-Accessible Control Infrastructure for Rapid FPGA Development**

*Andrew Heckerling*, Thomas Anderson, HuyTam Nguyen, Greg Price, Sara Siegal and John Thomas / MIT Lincoln Laboratory

**Transition to the Auditorium**

*Denotes Presenting Author*

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### 24 September (Continued)

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- 1145 **Poster / Demo B: Novel Computing Hardware**  
Chair: Peter Boettcher / MIT Lincoln Laboratory
- 1155 **Poster / Demo B Précis**
- Poster B.1**      **Resource-aware Distributed Block-based LU Decomposition on Wireless Sensor Networks**  
*Sherine Abdelhak*, Jared Tessier, Soumik Ghosh and Magdy Bayoumi / University of Louisiana at Lafayette
- Poster B.2**      **Application Implementation on the Cell B.E. Processor: Techniques Employed**  
*John Freeman*, Diane Brassaw, Rich Besler, Brain Few, Shelby Davis and Ben Buley / Black River Systems Company, Inc.
- Poster B.3**      **Embedding Constraint Satisfaction Using Parallel Soft-Core Processors on FPGAs**  
Prasad Subramanian and *Brandon Eames* / Utah State University
- Poster B.4**      **Hardware-in-the-Loop Simulation with the Common Simulation Framework**  
*Judith Gardiner* / Ohio Supercomputer Center
- Poster B.5**      **SmartCell: Architecture, Design and Performance Analysis for Reconfigurable Embedded Computing**  
*Xinming Huang* / Worcester Polytechnic Institute
- Poster B.6**      **Impact on High Performance Applications: FPGA Chip Bandwidth at 40 nm**  
*J. Ryan Kenny* / Altera Corporation
- Poster B.7**      **Implementation of a Highly Parameterized Digital PIV System On Reconfigurable Hardware**  
Abderrahmane Bennis, *Miriam Leeser* and Gilead Tadmor / Northeastern University  
Russ Tedrake / Massachusetts Institute of Technology
- Poster B.8**      **A Next-Generation Many-Core Processor with Reliability, Fault Tolerance and Adaptive Power Management Features Optimized for Embedded and High Performance Computing Applications**  
*Simon McIntosh-Smith* / ClearSpeed Technology plc
- Poster B.9**      **Converged Sensor Network Architecture (CSNA)**  
*Ian Dunn*, Michael Desrochers and Robert Cooper / Mercury Computer Systems, Inc.
- Poster B.10**      **NMP ST8 Dependable Multiprocessor (DM)**  
*John R. Samson, Jr.* / Honeywell International, Aerospace Systems
- Poster B.11**      **Threading Opportunities in High-Performance Flash-Memory Storage**  
*Craig Ulmer* / Sandia National Laboratories  
Maya Gokhale / Lawrence Livermore National Laboratory
- Poster B.12**      **Accelerating Floating Point DGEMM on FPGAs**  
Martin Langhammer and *Thomas VanCourt* / Altera Corporation
- 1230              **Lunch** (View Posters)

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### 24 September (Continued)

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|------|--|------|--|
| 1330 | <b>Session 4: Networking</b><br>Chair: Rick Pancoast / Lockheed Martin<br><b>Auditorium</b>  | 1330 | <b>Focus 4: Cell</b><br>Chair: Richard Linderman / AFRL<br><b>Room S2-180</b>  |
| 1340 | <b>Using Layer 2 Ethernet for High-Throughput, Real-Time Applications</b><br><i>Robert Blau</i> / Mercury Computer Systems, Inc.   | 1340 | <b>Synthetic Aperture Radar Backprojection on Sony PlayStation 3 Cell Broadband Engine and Intel Quad-core Xeon</b><br><i>Mark Backues</i> / SET Corporation<br>Uttam (Tom) Majumder / AFRL<br>Daniel York / SOCHE<br>Michael Minardi / AFRL |
| 1410 | <b>Performance and Energy Comparison of Electrical and Hybrid Photonic Networks for CMPs</b><br><i>Shoaib Kamil</i> / University of California at Berkeley, Lawrence Berkeley National Laboratory<br>Ankit Jain and Marghoob Mohiyuddin / University of California at Berkeley<br>John Shalf / Lawrence Berkeley National Laboratory<br>John Kubiatiowicz / University of California at Berkeley   | 1410 | <b>Large Multicore FFTs: Approaches to Optimization</b><br><i>Sharon Sacco</i> / MIT Lincoln Laboratory  |
| 1440 | <b>Invited: A Real-Time Publish-Subscribe Control Plane for a COTM Node</b><br>Darby Mitchell / MIT Lincoln Laboratory   | 1440 | <b>Optimizing Discrete Wavelet Transform on the Cell Broadband Engine</b><br><i>Seunghwa Kang</i> and David Bader / Georgia Institute of Technology  |
| 1510 | <b>Break</b> (View Posters)  |      | <b>Transition to the Auditorium</b>  |
| 1525 | <b>Panel: Paving the Way for Multicore Open Systems Architectures</b><br>Moderator: Dr. James C. Anderson / MIT Lincoln Laboratory<br><br><b>Distinguished Panelists:</b><br>Prof. Saman Amarasinghe / Massachusetts Institute of Technology CSAIL<br>Mr. Markus Levy / The Multicore Association and The Embedded Microprocessor Benchmark Consortium<br>Dr. Steve Muir / Vanu, Inc.<br>Mr. Matthew Reilly / SiCortex, Inc.<br>Mr. John Rooks / AFRL/RITC |      |  |
| 1700 | <b>Closing Remarks / Adjourn</b>   |      |  |

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### 25 September

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Announcements**

Mr. Robert Bond / MIT Lincoln Laboratory

0835 **Session 5: Innovative Software Tools**

Chair: Craig Lund / Independent Consultant  
Auditorium

0835 **Focus 5: Benchmarking**

Chair: John Gresh / Lawrence Livermore National  
Laboratory  
Room S2-180

0845 **PVTOL: Designing Portability, Productivity and Performance for Multicore Architectures**

*Hahn Kim*, Nadya Bliss, Jim Daly, Karen Eng, Jeremiah Gale, James Geraci, Ryan Haney, Jeremy Kepner, Sanjeev Mohindra, Sharon Sacco and Edward Rutledge / MIT Lincoln Laboratory

0845 **Evaluating the Productivity of a Multicore Architecture**

*Jeremy Kepner* and Nadya Bliss / MIT Lincoln Laboratory

0915 **Fixed and Reconfigurable Multi-Core Device Characterization for HPEC**

*Jason Williams*, Alan George, Justin Richardson, Kunal Gosrani and Siddarth Suresh / University of Florida

0915 **Parallelizing QR Decompositions with the R-Stream Compiler**

*Allen Leung*, Nicolas Vasilache, Benoît Meister and Richard Lethin / Reservoir Labs, Inc.

0945 **Runtime Performance Monitoring of Architecturally Diverse Systems**

*Joseph Lancaster* and Roger Chamberlain / Washington University in St. Louis

0945 **CrossCheck: Improving System Confidence through High-Speed Dynamic Property Checking**

*Jonathan Springer*, James Ezick and David Wohlford / Reservoir Labs, Inc. Matthew Craven and Rick Buskens / Lockheed Martin

Transition to the Auditorium

1015 **Break**

1030 **Simple, Efficient, Portable Decomposition of Large Data Sets**

*William Lundgren* / Gedae, Inc. David Erb and Max Aguilar / IBM Kerry Barnes and James Steed / Gedae, Inc.

1100 **Structural Object Programming Model: Enabling Efficient Development on Massively Parallel Architectures**

Laurent Bonetto, Brad Budlong, *Michael Butts* and Paul Wasson / Ambric, Inc.





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### 25 September (Continued)

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- 1130 **Poster / Demo C: Multicore Programming Environments**  
Chair: Craig Lund / Independent Consultant
- 1140 **Poster / Demo C Précis**
- Poster C.1**      **Rad Hard By Software for Space Multicore Processing**  
*David Bueno*, Dave Campagna, Dave Kessler and Eric Grobelny / Honeywell Inc.
- Poster C.2**      **Program Generation with Spiral: Beyond Transforms**  
*Franz Franchetti*, Daniel McFarlin, Frédéric de Mesmay, Hao Shen, Tomasz Wlodarczyk, Srinivas Chellappa, Marek Telgarsky, Peter Milder, Yevgen Voronenko, Qian Yu, James Hoe, José Moura and Markus Püschel / Carnegie Mellon University
- Poster C.3**      **A General Framework for Multicore Programming with Sourcery VSIPL++**  
*Brooks Moses*, Jules Bergmann, Stefan Seefeld, Don McCoy and Mike LeBlanc / CodeSourcery, Inc.
- Poster C.4**      **Measurement, Visualization, and Improvement of Linux Cluster Performance**  
Paul Howard, *Bruce Schulman* and Stephen Fried / Microway, Inc.
- Poster C.5**      **Partitioned FFTC: An Improved Fast Fourier Transform for the IBM Cell Broadband Engine**  
*Andrew Shaffer*, Bruce Einfalt and Padma Raghavan / Pennsylvania State University
- Poster C.6**      **Parallelization of NUFFT with Radial Data on Multicore Processors**  
Nikos Pitsianis and *Xiaobai Sun* / Duke University
- Poster C.7**      **LabVIEW Real Time for High Performance Control Applications**  
*Aljosa Vrancic* and Lothar Wenzel / National Instruments
- Poster C.8**      **An Approach Using the Data Distribution Service as the Connecting Transport for 100X Joint Battlespace Infosphere Servers**  
*Lei Zhao*, Douglas Blough, Vincent Mooney III and Justin Fiore / Georgia Institute of Technology
- 1225      **Lunch** (View Posters)

# High Performance Embedded Computing Workshop

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## AGENDA

### 25 September (*Continued*)

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- 1325 **Session 6: Awards Session**  
Chair: James Lebak / The MathWorks  
**Auditorium**
- 1335 ★ **Theory of Multicore Algorithms**  
*Jeremy Kepner* and Nadya Bliss / MIT Lincoln Laboratory
- 1405 ★ **GPU Performance Assessment with the HPEC Challenge**  
*Andrew Kerr*, Dan Campbell and Mark Richards / Georgia Institute of Technology
- 1435 ★ **Scalable SAR with Sourcery VSIPL++ for the Cell/B.E.**  
*Jules Bergmann*, Mike LeBlanc, Don McCoy, Brooks Moses and Stefan Seefeld / CodeSourcery, Inc.
- 1505 **Break** (View Posters)
- 1520 ★ **Language, Dialect, and Speaker Recognition Using Gaussian Mixture Models on the Cell Processor**  
*Nicolas Malyska*, Sanjeev Mohindra, Douglas Reynolds and Jeremy Kepner / MIT Lincoln Laboratory
- 1550 ★ **Generating High-Performance General Size Linear Transform Libraries Using Spiral**  
*Yevgen Voronenko*, Franz Franchetti, Frédéric de Mesmay and Markus Püschel / Carnegie Mellon University
- 1620 **Invited: The Next "Big Thing" for High Performance Embedded Computing: Cyber Security and Information Assurance**  
John Grosh / Lawrence Livermore National Laboratory
- 1650 **Awards**  
Jeremy Kepner / MIT Lincoln Laboratory
- 1700 **Adjourn**

★ Denotes outstanding submission

*Denotes Presenting Author*