High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

18 – 20 September

Workshop at a Glance

Day 1	Check-in / Setup:	0730
18 September	Welcome:	0830
		Keynote Addresses
		Opening Remarks
	Sessions:	**Session 1:** Multicore Technologies
		Poster / Demo A: Advanced Algorithms and Hardware
		Session 2: Runtime Optimization
		Focus 2: US ONLY
		(Session 2 and Focus 2 run in parallel)
	Adjourn:	1700
		1800 **Reception**
		1845 **Banquet Speaker**
		1930 **Banquet**

Day 2	Check-in / Setup:	0730
19 September	Announcements:	0830
	Sessions:	**Session 3:** Multicore Hardware Challenges
		Focus 3: Cell
		(Session 3 and Focus 3 run in parallel)
		Poster / Demo B: FPGA Technologies and Applications
		Session 4: Novel Applications
		Focus 4: GPUs
		(Session 4 and Focus 4 run in parallel)
		Panel: Multicore Meltdown?
	Adjourn:	1715

Day 3	Check-in / Setup:	0730
20 September	Announcements:	0830
	Sessions:	**Session 5:** Multicore Environments
		Focus 5: Benchmarking
		(Session 5 and Focus 5 run in parallel)
		Poster / Demo C: Cell / GPU Technologies
		Session 6: Awards Session
	Adjourn:	1730

High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

18 September

Day 1 at a Glance

0730	**Check-in / Poster Setup / Continental Breakfast**		
0830	**Welcome:** Mr. David Martinez / MIT Lincoln Laboratory		
0835	**Mission Keynote Speaker:** Dr. Michael McGrath / DASN (RDT & E)		
0905	**Technology Keynote Speaker:** Prof. Jack Dongarra / University of Tennessee, ICL		
0935	**Opening Remarks:** Mr. Robert Bond / MIT Lincoln Laboratory		
	Auditorium		**Room S2-180**
0940	**Session 1:** Multicore Technologies		
0945	Invited Speaker: Saman Amarasinghe / Massachusetts Institute of Technology CSAIL		
1015	**Break**		
1030	Kenneth Prager / Raytheon Company		
1100	Invited Speaker: Hans Zima / Jet Propulsion Laboratory, California Institute of Technology; Institute of Scientific Computing, University of Vienna, Austria		
1130	**Poster / Demo A:** Advanced Algorithms and Hardware		
1225	**Lunch** (View Posters)		
1345	**Session 2:** Runtime Optimization	**1345**	**Focus 2:** US ONLY
1355	Albert Reuther / MIT Lincoln Laboratory		
1425	Daniel Waddington / Lockheed Martin Corporation		
1455	Dong-In Kang / University of Southern California, ISI		
1525	**Break** (View Posters)		
1550	Invited Speaker: David Scott / Intel Corporation		
1620	Invited Speaker: Zachary Lemnios / MIT Lincoln Laboratory		
1650	**Closing Remarks:** Jeremy Kepner / MIT Lincoln Laboratory		
1700	**Adjourn**		
1800	**Reception**		
1845	**Banquet Speaker:** Mr. Doug Malewicki / AeroVisions, Inc.		
1930	**Banquet**		

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Welcome**
Mr. David Martinez / MIT Lincoln Laboratory

0835 **Mission Keynote Speaker: Convergence of C2 and Combat System – Leveraging SOA**
Dr. Michael McGrath / DASN (RDT & E)

0905 **Technology Keynote Speaker: The Impact of Multicore on Math Software**
Prof. Jack Dongarra / University of Tennessee, ICL

0935 **Opening Remarks**
Mr. Robert Bond / MIT Lincoln Laboratory

0940 **Session 1: Multicore Technologies**
Chair: Michael Vai / MIT Lincoln Laboratory
Auditorium

0945 **StreamIt—A Programming Language for the Era of Multicores**
Saman Amarasinghe / Massachusetts Institute of Technology CSAIL

1015 **Break** (View Posters)

1030 **World's First Polymorphic Computer—MONARCH**
Lloyd Lewins, Kenneth Prager, Gillian Groves and Michael Vahey / Raytheon Company

1100 **Advanced Programming and Execution Models for Future Multi-Core Systems**
Hans Zima / Jet Propulsion Laboratory, California Institute of Technology; Institute of Scientific Computing, University of Vienna, Austria

High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

18 September *(Continued)*

1130 **Poster / Demo A: Advanced Algorithms and Hardware**
Chair: Michael Vai / MIT Lincoln Laboratory

1140 **Poster / Demo A Précis**

Poster A.1 **ALPS: Software Framework for Scheduling Parallel Computations with Application to Parallel Space-Time Adaptive Processing**
Kyusoon Lee and Adam Bojanczyk / Cornell University

Poster A.2 **A Clustered Multiprocessor and Its Multicore Building Block**
Matthew Reilly / SiCortex, Inc.

Poster A.3 **NMP ST8 Dependable Multiprocessor**
John Samson, Jr. / Honeywell, Inc.
Alan George / University of Florida
Rafi Some / Jet Propulsion Laboratory, California Institute of Technology

Poster A.4 **DMAGIC: A High-level Partitioning Methodology for Discrete Signal Transforms onto Distributed Hardware Architectures**
Rafael Arce-Nazario, Manuel Jiménez and Domingo Rodríguez / University of Puerto Rico, Mayagüez

Poster A.5 **TeraByte TokuSampleSort**
Bradley Kuszmaul / Massachusetts Institute of Technology CSAIL, Tokutek Inc., Cilk Arts Inc., and MIT Lincoln Laboratory

Poster A.6 **Use of Dense Wavelength Division Multiplexing (DWDM) Optical Interconnects to Improve Parallel and Distributed Processing Architecture Connectivity**
Rick Stevens, Greg Whaley, Roger Karnopp, Howard Schantz and Mert Horne / Lockheed Martin Corporation

Poster A.7 **Performance of Direct Attached Disk Subsystems**
Roger Chamberlain / Washington University in St. Louis and Exegy, Inc.
Berkley Shands / Washington University in St. Louis

Poster A.8 **When Storage Devices Become Computers**
Robert Thibadeau and *Kevin Gomez / Seagate Research
Tom Mitchell and David Touretzky / Carnegie Mellon University
Terrence Sejnowski / Salk Institute

Poster A.9 **Low Latency Real-Time Computing on Multiprocessor Systems Running Standard Linux**
Dimitri Sivanich / SGI

Poster A.10 **Optimization of Memory Allocation in VSIPL**
Jinwoo Suh, Janice McMahon, Stephen Crago and Dong-In Kang / University of Southern California, ISI

Poster A.11 **Use of Python as a Matlab Replacement for Algorithm Development and Execution in a Multi-Core Environment**
Glen Mabey / Southwest Research Institute
Brian Granger / Tech-X Corporation

Poster A.12 **Automatic Deployment of Streaming Applications on Hybrid Architectures**
Roger Chamberlain and Mark Franklin / Washington University in St. Louis

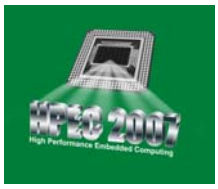
Poster A.13 **Multiprocessor Implementation of a Face Detection System**
Sankalita Saha / University of Maryland, College Park
Neal Bambha / US Army Research Laboratory
*Shuvra Bhattacharyya / University of Maryland, College Park

Poster A.14 **Synthesizing Parallel Programming Models for Asymmetric Multi-core Systems**
Dimitrios Nikolopoulos and Kirk Cameron / Virginia Tech

Poster A.15 **Benchmarking Publish/Subscribe Middleware for Radar Applications**
Andrew Rhoades, Glenn Schrader and Paul Poulin / MIT Lincoln Laboratory

1225 **Lunch** (View Posters)

*** Denotes presenter other than first listed author**



High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

18 September *(Continued)*

1345 **Session 2: Runtime Optimization**
Chair: Joel Goodman / MIT Lincoln Laboratory
Auditorium

1355 **TX-2500—An Interactive, On-Demand Rapid-Prototyping HPC System**
Albert Reuther, Bill Arcand, Tim Currie, Andy Funk, Jeremy Kepner, Matthew Hubbell, Andrew McCabe and Peter Michaleas / MIT Lincoln Laboratory

1425 **Thimble: Design-time Analysis of Multi-threaded System Behavior**
Daniel Waddington / Lockheed Martin Corporation

1455 **Preliminary Study toward Intelligent Run-time Resource Management Techniques for Large Multi-Core Architectures**
Dong-In Kang, Jinwoo Suh, Janice McMahon and Stephen Crago / University of Southern California, ISI

1525 **Break** (View Posters)

1550 **HPC Processor Trends from High-end to Volume, Small, Large, Open, or Embedded**
David Scott / Intel Corporation

1620 **Research Challenges for the Next Decade**
Zachary Lemnios / MIT Lincoln Laboratory

1650 **Closing Remarks**
Jeremy Kepner / MIT Lincoln Laboratory

1700 **Adjourn**

1800 **Reception**

1845 **Banquet Speaker: American Innovator**
Mr. Doug Malewicki / AeroVisions, Inc.

1930 **Banquet**

1345 **Focus 2: US Only**
Chair: Rick Pancoast / Lockheed Martin Corp.
Room S2-180

Transition to the Auditorium

High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

19 September

Day 2 at a Glance

0730 **Check-in / Poster Setup / Continental Breakfast**
0830 **Announcements:** Mr. Robert Bond / MIT Lincoln Laboratory

	Auditorium	**Room S2-180**
0835	**Session 3:** Multicore Hardware Challenges	
0845	Invited Speaker: Anant Agarwal / Massachusetts Institute of Technology CSAIL	
0915	Invited Speaker: James Held / Intel Corporation	
0945	Invited Speaker: Markus Levy / The Multicore Association and The Embedded Microprocessor Benchmark Consortium	
1015	**Break**	
1030	Yongfeng Gu / Boston University	**1030** **Focus 3:** Cell
		1040 David Bader / Georgia Institute of Technology
1100	Peter Vouras / The Johns Hopkins University	
		1110 Richard Besler / Black River Systems Company
1130	**Poster / Demo B:** FPGA Technologies and Applications	
		1140 Frank Lauginiger / Mercury Computer Systems, Inc.
1235	**Lunch** (View Posters)	
1335	**Session 4:** Novel Applications	**1335** **Focus 4:** GPUs
1345	Sharon Sacco / MIT Lincoln Laboratory	**1345** Invited Speaker: Norman Rubin / ATI Research
1415	Mark Duchaineau / Lawrence Livermore National Laboratory	**1415** Douglas Enright / The Aerospace Corporation
1445	Nadya Travinin Bliss / MIT Lincoln Laboratory	**1445** Xiaobai Sun / Duke University
1515	**Break** (View Posters)	**1515** Dennis Braunreiter / SAIC
1545	**Panel:** Dr. James C. Anderson / MIT Lincoln Laboratory	
1715	**Adjourn**	

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Announcements**
Mr. Robert Bond / MIT Lincoln Laboratory

0835 **Session 3: Multicore Hardware Challenges**
Chair: Robert Bond / MIT Lincoln Laboratory
Auditorium

0845 **The Tile Processor: A 64-Core Multicore for Embedded Processing**
Anant Agarwal / Massachusetts Institute of Technology CSAIL

0915 **Intel™ 80-core Tera-scale Research Processor**
James Held / Intel Corporation

0945 **Using Industry Standards to Exploit the Advantages and Resolve the Challenges of Multicore Technology**
Markus Levy / The Multicore Association and
The Embedded Microprocessor Benchmark Consortium

1015 **Break**

1030 **Amenability of Multigrid Computations to FPGA-Based Acceleration**
Yongfeng Gu and *Martin Herbordt / Boston University

1100 **High Performance Parallel Implementation of Adaptive Beamforming using Sinusoidal Dithers**
Peter Vouras and Trac Tran / The Johns Hopkins University

1030 **Focus 3: Cell**
Chair: Sharon Sacco / MIT Lincoln Laboratory
Room S2-180

1040 **FFTC: Fastest Fourier Transform for the IBM Cell Broadband Engine**
David Bader and *Virat Agarwal / Georgia Institute of Technology

1110 **Implementation of SIGINT Application on CELL-BE**
Richard Besler / Black River Systems Company
Emily Krzysiak / Air Force Research Laboratory

1140 **Performance of a Multicore Matrix Multiplication Library**
Frank Lauginiger, Robert Cooper, Jonathan Greene, Michael Pepe and Myra Jean Prelle / Mercury Computer Systems, Inc.

*** Denotes presenter other than first listed author**

High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

19 September *(Continued)*

1130 **Poster / Demo B: FPGA Technologies and Applications**
Chair: Robert Bond / MIT Lincoln Laboratory

1140 **Poster / Demo B Précis**

Poster B.1 **Evaluating Partial Reconfiguration for Embedded FPGA Applications**
Ross Hymel, Alan George, *Chris Conger and Herman Lam / University of Florida

Poster B.2 **A Streaming FFT on 3GSPS ADC Data using Core Libraries and DIME-C**
Robin Bruce / Institute of System Level Integration, Alba Centre
*Malachy Devlin / Nallatech

Poster B.3 **Accelerating Algorithm Implementation in FPGA/ASIC Using Python**
Tom Dillon, Jeremy Paatela, Guenter Dannoritzer and Scott Hussong / Dillon Engineering, Inc.

Poster B.4 **Phase Unwrapping on Reconfigurable Hardware**
Sherman Braganza and Miriam Leeser / Northeastern University

Poster B.5 **SmartCell: A Coarse-Grained Reconfigurable Architecture for High Performance and Low Power Embedded Computing**
Xinming Huang / Worcester Polytechnic Institute

Poster B.6 **Accelerating Genome Sequencing 100X with FPGAs**
Olaf Storaasli / Oak Ridge National Laboratory

Poster B.7 **Prototyping Advanced Military Sensor Systems Using FPGA-to-ASIC Design Flow**
J. Ryan Kenny and Jeff Wills / Altera Corporation
Rick Pancoast and Ellis Taliaferro / Lockheed Martin Corporation

Poster B.8 **Digital Beam Former Coefficient Management Using Advanced Embedded Processor Technology**
J. Ryan Kenny and Argy Krikelis / Altera Corporation

Poster B.9 **FPGA Coprocessing in Multi-Core Architectures for DSP**
J. Ryan Kenny and Bryce Mackin / Altera Corporation

Poster B.10 **Transformation of Sequential Software into Parallel FPGA Hardware: A Case Study Using the SPEC CPU 2006 Benchmarks**
Raymond Hoare / Concurrent EDA, LLC

Poster B.11 **FPGA-Based Acceleration of an Image Registration Algorithm**
Jay Brockman, Daniel Rinzler and Peter Bui / University of Notre Dame
Frank Iannarilli / Aerodyne Research, Inc.

Poster B.12 **Applying Open Standards to FPGA IP Interfaces**
Shepard Siegel / Mercury Computer Systems, Inc.

Poster B.13 **FPGA Based Systolic Array Implementation of QR Transformation Using Givens Rotations**
Xiaojun Wang and Miriam Leeser / Northeastern University

1235 **Lunch** (View Posters)

*** Denotes presenter other than first listed author**

19 September *(Continued)*

1335 **Session 4: Novel Applications**
Chair: David Cousins / BBN Technologies
Auditorium

1345 **Projective Transform on Cell: A Case Study**
Sharon Sacco, Hahn Kim, Sanjeev Mohindra, Peter Boettcher, Chris Bowen, Nadya Travinin Bliss, Glenn Schrader and Jeremy Kepner / MIT Lincoln Laboratory

1415 **Toward Fast Computation of Dense Image Correspondence on the GPU**
Mark Duchaineau, Jonathan Cohen and Sheila Vaidya / Lawrence Livermore National Laboratory

1445 **Analysis and Mapping of Sparse Matrix Computations**
Nadya Travinin Bliss and Sanjeev Mohindra / MIT Lincoln Laboratory
Varun Aggarwal / Massachusetts Institute of Technology
Una-May O'Reilly / Massachusetts Institute of Technology CSAIL

1515 **Break** (View Posters)

1545 **Panel: Multicore Meltdown?**
Moderator: Dr. James C. Anderson / MIT Lincoln Laboratory

Distinguished Panelists:
Dr. James Held / Intel Corporation
Mr. Markus Levy / The Multicore Association and The Embedded Microprocessor Benchmark Consortium
Mr. Greg Rocco / Mercury Computer Systems, Inc.
Mr. Kalpesh Sheth / Advanced Processing Group, DRS Technologies
Dr. Thomas VanCourt / Altera Corporation

1715 **Closing Remarks / Adjourn**

1335 **Focus 4: GPUs**
Chair: Craig Lund / Mercury Computer Systems
Room S2-180

1345 **Are Graphics Processors the New Supercomputers?**
Norman Rubin / ATI Research

1415 **Benchmarking the NVIDIA 88006TX with the CUDA Development Platform**
Michael McGraw-Herdeg / Massachusetts Institute of Technology
*Douglas Enright and B. Scott Michel / The Aerospace Corporation

1445 **FFTs of Arbitrary Dimensions on GPUs**
Xiaobai Sun and Nikos Pitsianis / Duke University

1515 **DARPA Strap-Boy: Fast Hybrid QR-Cholesky Factorization and Tuning Techniques for STAP Algorithm Implementation on Graphics Processor Architectures for Embedded Systems**
Dennis Healy / DARPA
*Dennis Braunreiter, Jackie Sillaci, David Boe and Jeremy Furtek / SAIC
Xaiobai Sun / Duke University

Transition to the Auditorium

*** Denotes presenter other than first listed author**

High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

20 September

Day 3 at a Glance

0730 **Check-in / Poster Setup / Continental Breakfast**
0830 **Announcements:** Mr. Robert Bond / MIT Lincoln Laboratory

Auditorium

0835 **Session 5:** Multicore Environments
0845 James Geraci / Massachusetts Institute of Technology
0915 Jules Bergmann / CodeSourcery
0945 William Lundgren / Gedae, Inc.
1015 **Break**
1030 Hahn Kim / MIT Lincoln Laboratory
1100 Thomas Steck / Lockheed Martin Corporation
1130 **Poster / Demo C:** Cell / GPU Technologies
1235 **Lunch** (View Posters)
1345 **Session 6:** Awards Session
1355 Nicholas Moore / Northeastern University
1425 Keren Bergman / Columbia University
1455 **Break** (View Posters)
1520 Jeffrey Rudin / Mercury Computer Systems, Inc.
1550 Dong Hyuk Woo / Georgia Institute of Technology
1620 Invited Speaker: Matteo Frigo / Cilk Arts
1650 **Awards:** Jeremy Kepner / MIT Lincoln Laboratory
1730 **Adjourn**

Room S2-180

1030 **Focus 5:** Benchmarking
1040 Chris Conger / University of Florida
1110 Justin Tripp / Los Alamos National Laboratory
1140 Ray Artz / Lockheed Martin Corporation

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Announcements**
Mr. Robert Bond / MIT Lincoln Laboratory

0835 **Session 5: Multicore Environments**
Chair: Robert Bond / MIT Lincoln Laboratory
Auditorium

0845 **High Performance Simulations of Electrochemical Models on the Cell Broadband Engine**
James Geraci and Sudarshan Raghunathan /
Massachusetts Institute of Technology

0915 **Sourcery VSIPL++ for the Cell/B.E.**
Jules Bergmann, Mark Mitchell, Don McCoy,
Stephan Seefeld and Assem Salama / CodeSourcery
Fred Christensen / IBM
Rick Pancoast and Thomas Steck /
Lockheed Martin Corporation

0945 **Programming Examples that Expose Efficiency Issues for the Cell Broadband Engine Architecture**
William Lundgren / Gedae, Inc.
Rick Pancoast / Lockheed Martin Corporation
David Erb / IBM
Kerry Barnes and James Steed / Gedae, Inc.

1015 **Break**

20 September *(Continued)*

1030 **PVTOL: A High-Level Signal Processing Library for Multicore Processors**
Hahn Kim, Nadya Travinin Bliss, Ryan Haney, Jeremy Kepner, Sanjeev Mohindra, Sharon Sacco, Glenn Schrader and Edward Rutledge / MIT Lincoln Laboratory

1100 **Defense Applications Implemented Utilizing the Parallel Processing Features of Sourcery VSIPL++**
Thomas Steck, Rick Pancoast and Ellis Taliaferro / Lockheed Martin Corporation
Jules Bergmann / CodeSourcery

1030 **Focus 5: Benchmarking**
Chair: James Lebak / The MathWorks
Room S2-180

1040 **Application-Level Benchmarking with Synthetic Aperture Radar**
Chris Conger, Adam Jacobs and Alan George / University of Florida

1110 **A Survey of Multi-Core Coarse-Grained Reconfigurable Arrays for Embedded Applications**
Justin Tripp, Jan Frigo and Paul Graham / Los Alamos National Laboratory

1140 **Exploring Multi-core Processors using Realistic Signal- and Image-processing Application Benchmarks**
Ray Artz, Brian Loe and Janet Pavelich / Lockheed Martin Corporation
Jules Bergmann / CodeSourcery

High Performance Embedded Computing Workshop

18 – 20 September 2007

AGENDA

20 September *(Continued)*

1130 **Poster / Demo C: Cell / GPU Technologies**
Chair: Robert Bond / MIT Lincoln Laboratory

1140 **Poster / Demo C Précis**

Poster C.1 **Hardware and Compute Abstraction Layers for Accelerated Computing Using Graphics Hardware and Conventional CPUs**
Justin Hensley / Advanced Micro Devices, Inc.

Poster C.2 **Gedae Portability: From Simulation to DSPs to the Cell Broadband Engine**
James Steed, William Lundgren and Kerry Barnes / Gedae, Inc.

Poster C.3 **Accelerating MATLAB with CUDA**
Massimiliano Fatica / NVIDIA Corporation
Won-Ki Jeong / University of Utah

Poster C.4 **Implementation of Parallel Processing Techniques on Graphical Processing Units**
Brad Baker, Wayne Haney and Charles Choi / General Dynamics

Poster C.5 **R-Verify™: Deep Checking of Embedded Code**
James Ezick, Donald Nguyen and Richard Lethin / Reservoir Labs, Inc.
Rick Pancoast / Lockheed Martin Corporation

Poster C.6 **Dependable Multiprocessing with the Cell Broadband Engine**
David Bueno, Matt Clark and John Samson, Jr. / Honeywell, Inc.
Adam Jacobs / University of Florida

Poster C.7 **Chirp Radar Parameter Estimators over Distributed Hardware Structures**
Cesar Aceros-Moreno, Ana Ramirez and Domingo Rodriguez / University of Puerto Rico, Mayagüez

Poster C.8 **Introduction of Error Correcting Schemes in the Design Process of Self-Healing Circuits for Nanoscale Fabrics**
Catherine Dežan / Université de Bretagne Occidentale
*Teng Wang / University of Massachusetts

Poster C.9 **The Development and Performance Analysis of a Distributed Corner Turn using the AXIS Graphical Software System**
Thomas Litrenta / Radstone Embedded Systems

Poster C.10 **Multi-core Programming Frameworks for Embedded Multimedia Applications**
Kaushal Sanghai and Rick Gentile / Analog Devices, Inc.

Poster C.11 **Real-time Multi-core PDE-Solvers in LabVIEW**
Shawn McCaslin, Michael Cerna, Michael Chen, Nanxiong Zhang, Bin Wang and Lothar Wenzel / National Instruments

Poster C.12 **Announcing PWRficient Processors from PA Semi, the Most Power-Efficient, High-Performance Processors Available**
Pete Bannon / P.A. Semi

Poster C.13 ★ **Efficient Memorization Strategies for Object Recognition with a Multi-Core Architecture**
George Viamontes, Mohammed Amduka, Jon Russo, Matthew Craven and Thanh Vu Nguyen /
Lockheed Martin Corporation

1235 **Lunch** (View Posters)

★ **Denotes outstanding submission**
*** Denotes presenter other than first listed author**

20 September *(Continued)*

1345 **Session 6: Awards Session**
Chair: Jeremy Kepner / MIT Lincoln Laboratory
Auditorium

1355 ★ **Vforce: Aiding the Productivity and Portability in Reconfigurable Supercomputer Applications via Runtime Hardware Binding**
Nicholas Moore and Miriam Leeser / Northeastern University
Laurie Smith King / College of the Holy Cross

1425 ★ **On-Chip Photonic Communication for High-Performance Multi-Core Processors**
Keren Bergman and Luca Carloni / Columbia University

1455 **Break** (View Posters)

1520 ★ **Implementation of Polar Format SAR Image Formation on the IBM Cell Broadband Engine**
Jeffrey Rudin / Mercury Computer Systems, Inc.

1550 ★ **POD: A Parallel-On-Die Architecture**
Dong Hyuk Woo / Georgia Institute of Technology
Joshua Fryman / Intel Corporation
Allan Knies / Georgia Institute of Technology
Marsha Eng / Intel Corporation
Hsien-Hsin Lee / Georgia Institute of Technology

1620 **Multithreaded Programming in Cilk**
Matteo Frigo / Cilk Arts

1650 **Awards**
Jeremy Kepner / MIT Lincoln Laboratory

1730 **Adjourn**

★ **Denotes outstanding submission**