Advanced Hardware and Software Technologies for Ultra-long FFT's

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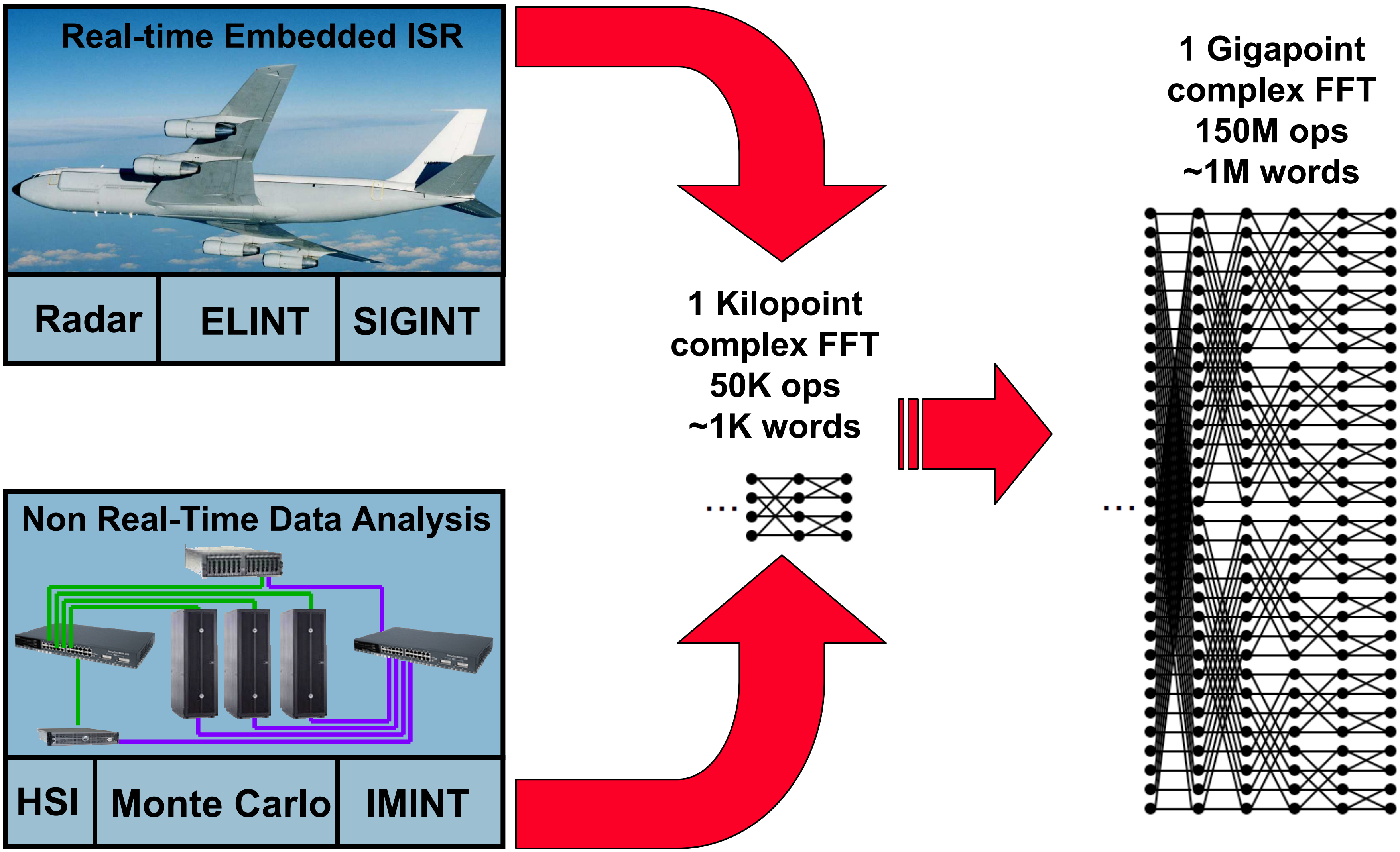
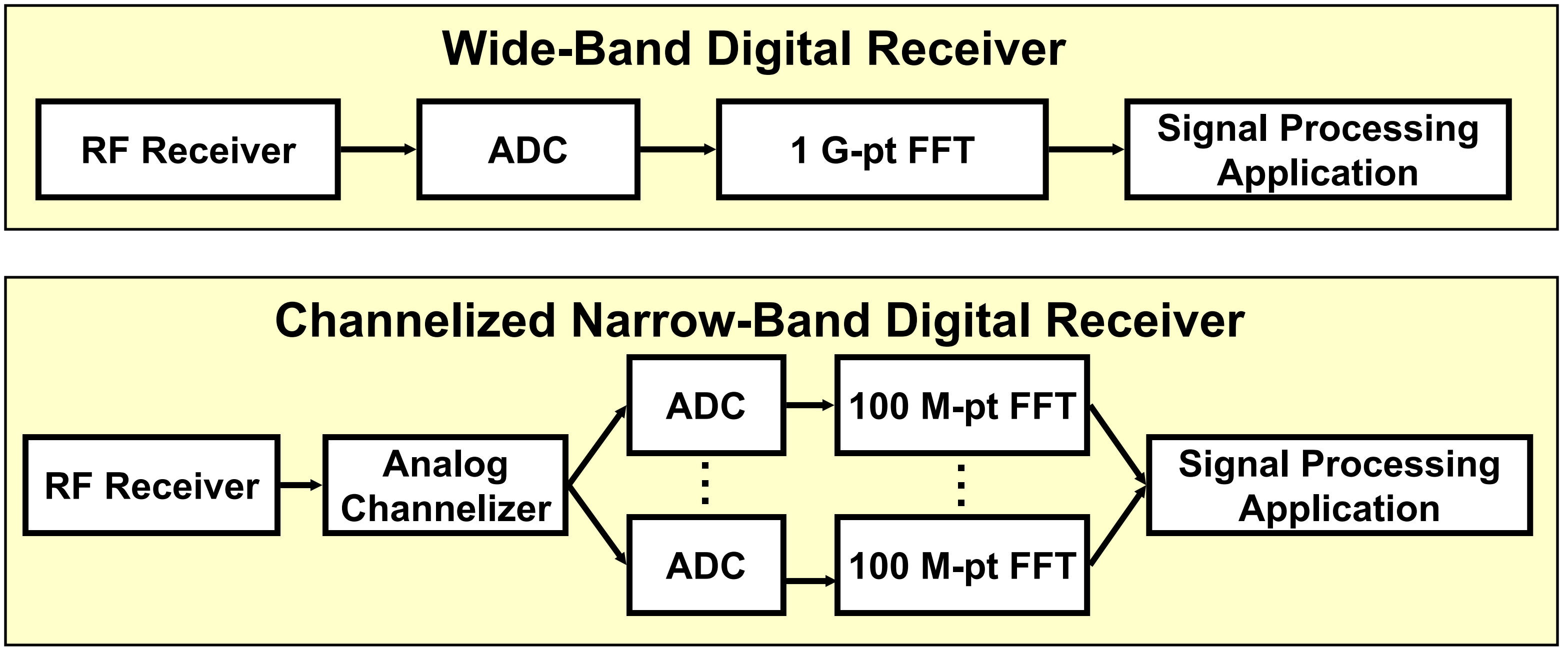
Outline

- **Background**
- **FPGA-Based Hardware Technology**
- **Parallel Software Technology**
- **Conclusions**

Introduction

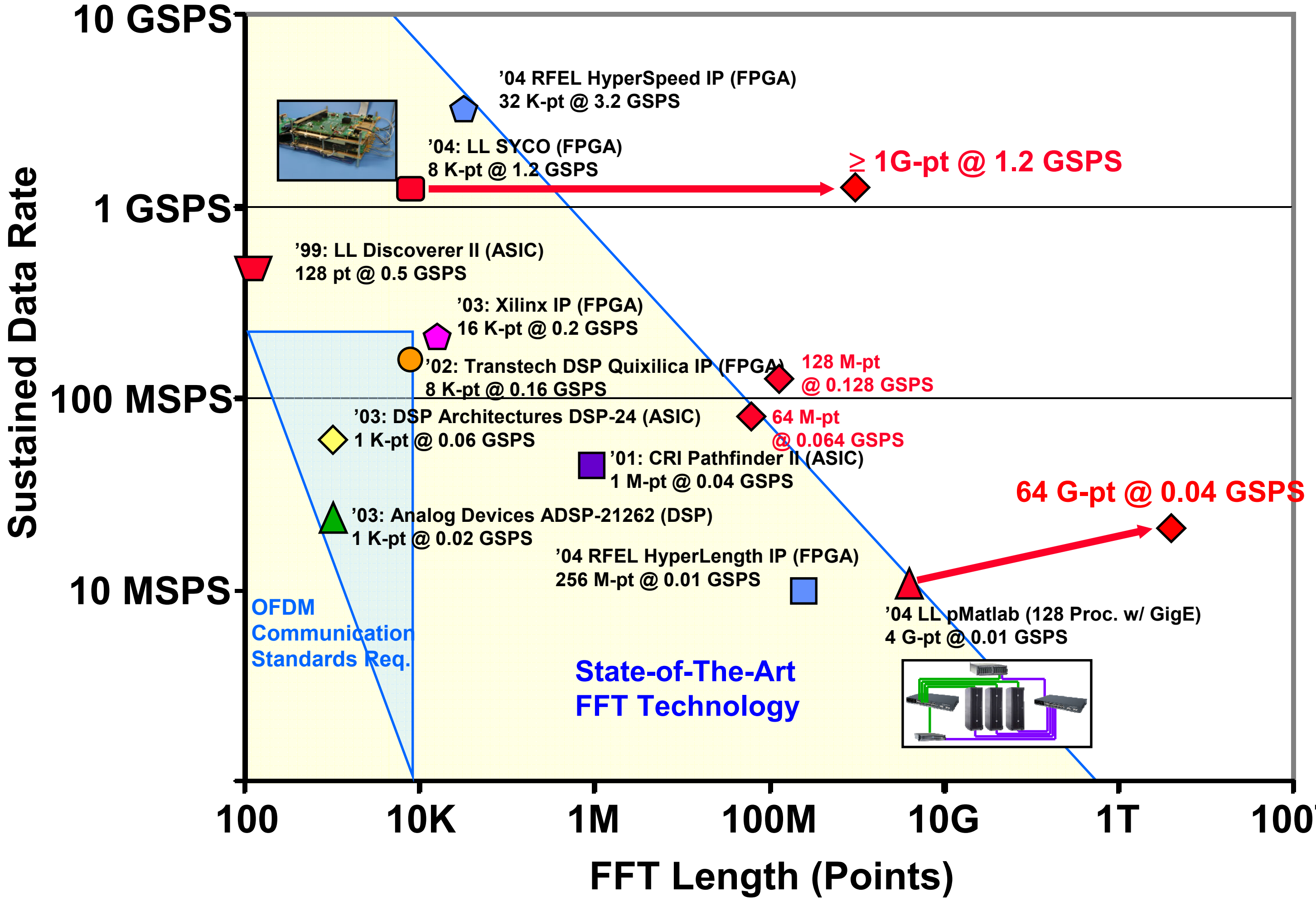


Motivation for Real-time, Ultra-long FFT's



- Can use FFT to detect weak signals
  - Reduce noise floor
  - Longer intervals result in higher gain
- Real-time, ultra-long FFT processor is a critical enabling component

FFT Technology Space



Objective: Extend state-of-the-art to ultra-long FFT's

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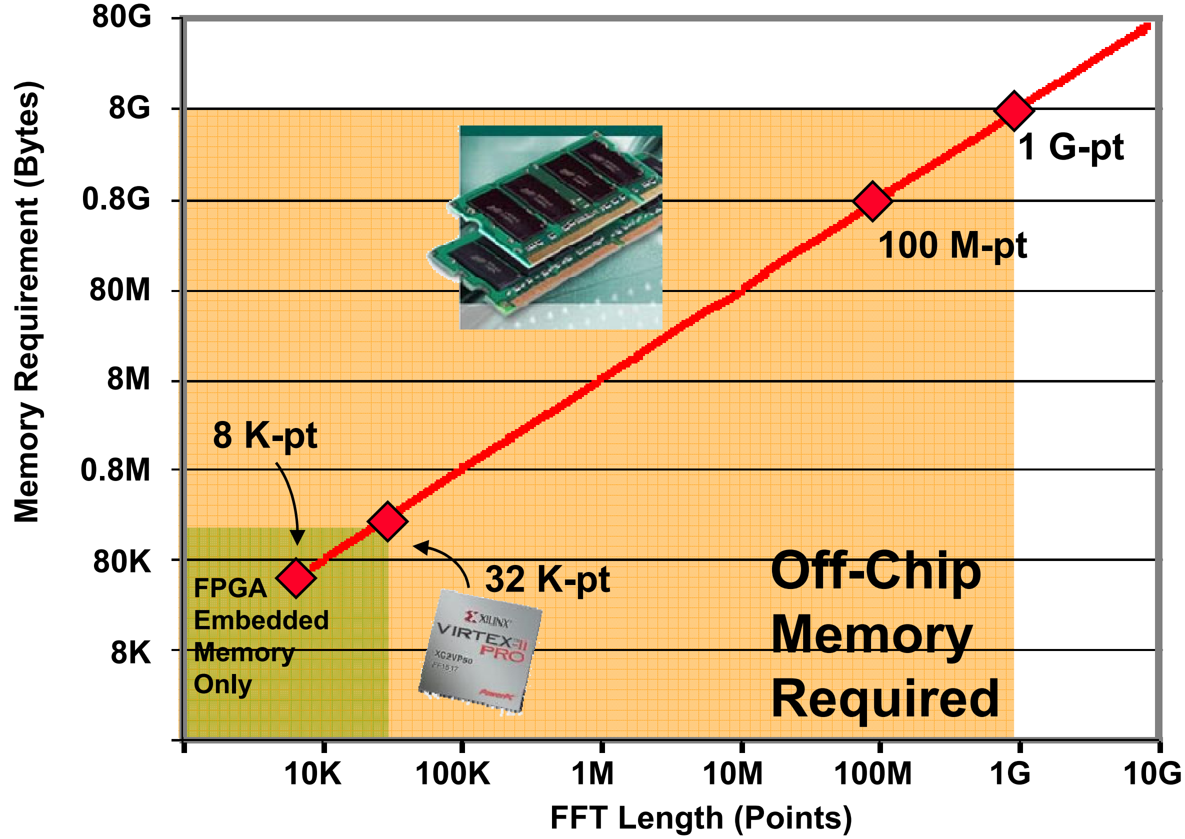
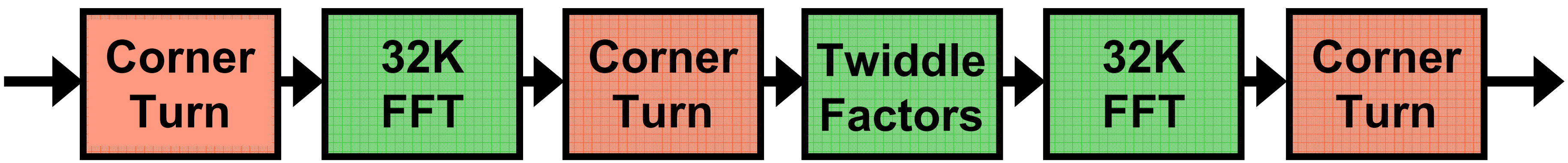
Ultra-long FFT Implementation Challenges



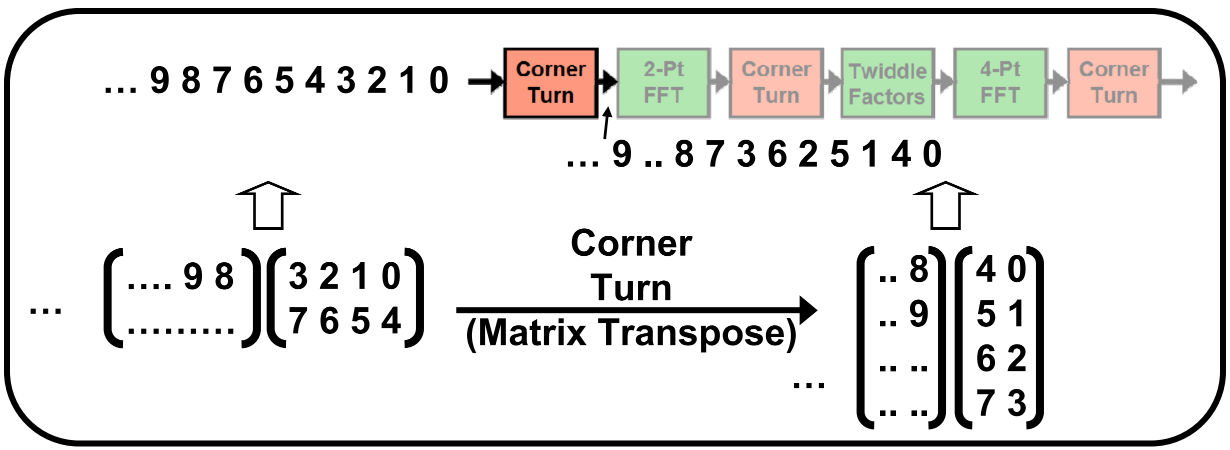
- Beyond ~32 K-pt FFT, off-chip memory for FIFO and twiddle factors is required
  - Full duplex memory access is a challenge
- Lincoln architecture selected for ultra-long FFT
  - "A Systolic FFT Architecture for Real Time FPGA Systems," *HPEC 2004*.

Real-Time 1G-Point FFT Architecture

- MN-pt FFT can be implemented with an M-pt FFT and an N-pt FFT
  - E.g. 1 G-pt FFT ⇒ M = 32 K-pt, N = 32 K-pt
  - Each 32 K-pt FFT fits into an FPGA



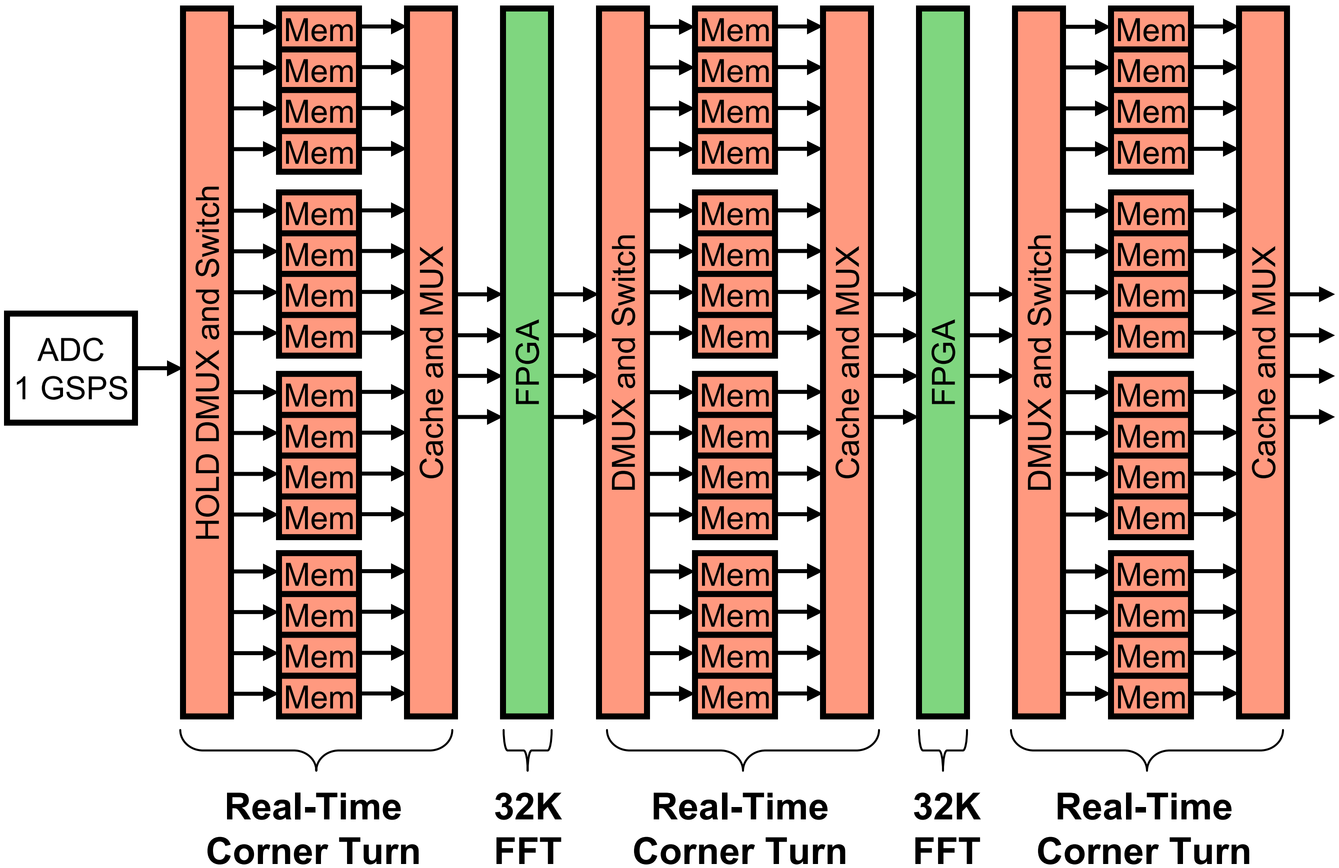
Corner Turn Example (for an 8-Point FFT):



- Lincoln has developed a corner turn architecture that operates at 1 GSPS

Real-Time FFT Architecture

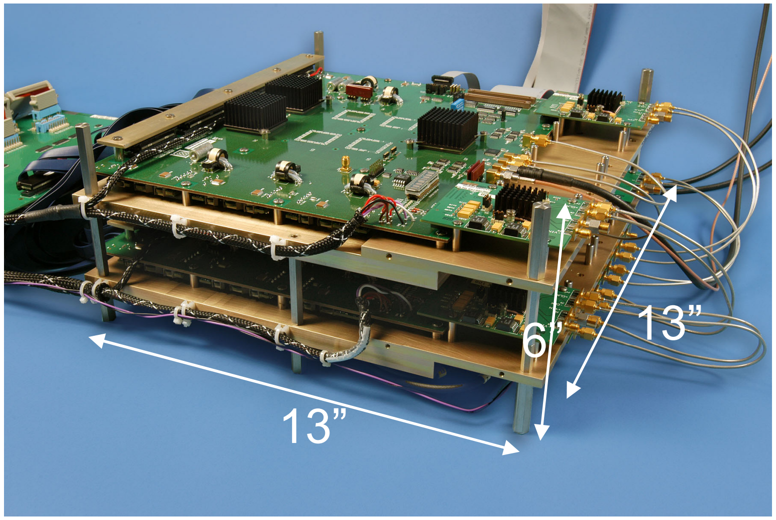
1 Gigapoint FFT Configuration



Reconfigurable architecture allows for multiple implementations:
e.g. 1 G-pt @ 1 GSPS or **100 M-pt @ 100 MSPS X 10 channels**

Real-time Example FFT Implementation

Current FFT Capabilities



- Symbiotic Communications (SYCO) real-time processor
  - 8 K-pt FFT
  - 450 GOPS @ 130 Watts
  - 208 FFT butterflies
  - No on-board memory
- "Rapid Prototyping of a Real-time Range Compression Processor," *HPEC 2005 Poster Session*

Future Ultra-long FFT Capabilities

- Processor enhancement
  - Provides on-board memory banks for performing real-time corner turns
  - Performs form-factor optimization
- Develop a universal FFT architecture
  - 100M-Pt FFT X 10 channels
  - 1G-Pt FFT

* Initial estimate based on double-precision operation

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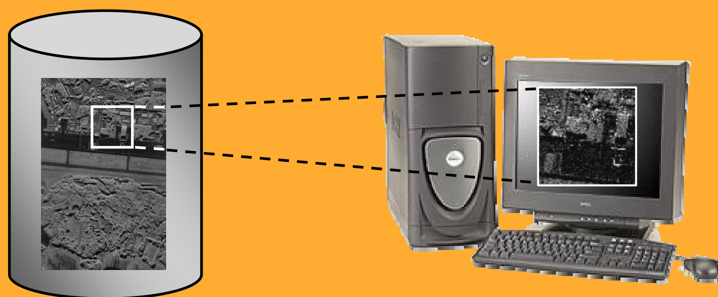
Motivation for Out-of-Core Technology

- **Data are often larger than memory on a single processor.**

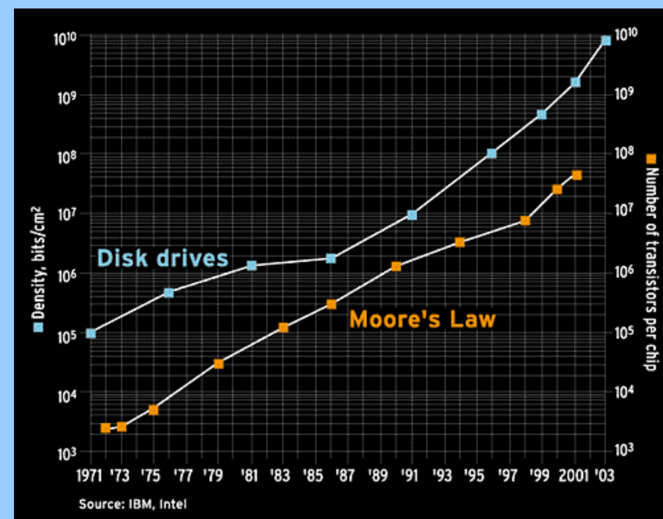
Memory



Can address memory limitation with:

1. **Multiple CPUs**
2. **Using disk as memory**

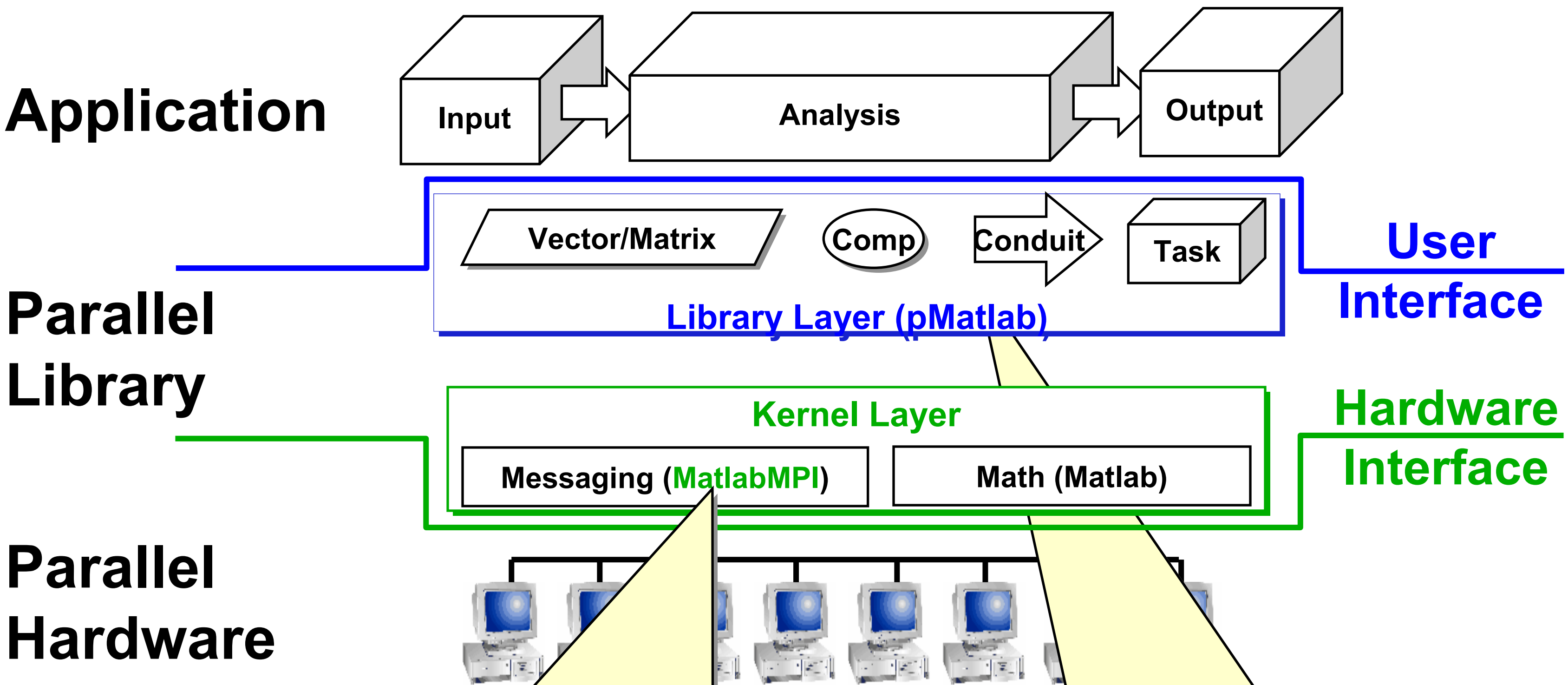
Disk



Hughes, G.F. "Wise Drives." IEEE Spectrum. Aug 2002.

- **Out-of-core technology uses memory as a "window" into data stored on disk.**

MatlabMPI & pMatlab Software Layers



- Can build a parallel library with a few messaging primitives
- MatlabMPI provides this messaging capability:

```
MPI_Send(dest,comm,tag,X);
X = MPI_Recv(source,comm,tag);
```

- Can build a application with a few parallel structures and functions
- pMatlab provides parallel arrays and functions

```
X = ones(n,mapX);
Y = zeros(n,mapY);
Y(:,:) = fft(X);
```

Out-of-Core Memory Management: pMatlab eXtreme Virtual Memory (XVM)

Virtual Memory

+ Transparent to user (ease of use)
– Disk access patterns are often sub-optimal for most algorithms

Out-of-Core

+ Provides control of disk at object level (performance)
– Exposes swapping mechanism to user

Goal of pMatlab XVM is to add out-of-core capability to pMatlab that is:

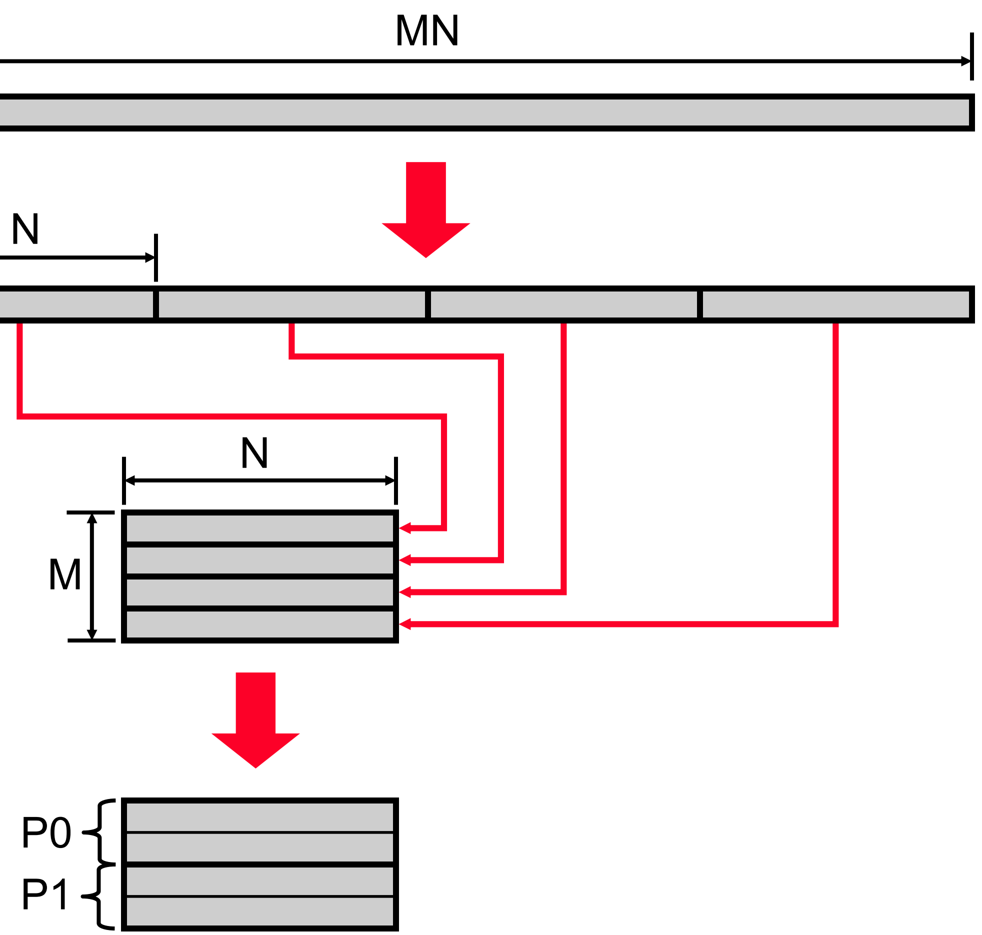
1. Easy to use
2. Has high performance
3. Can transparently distribute data

pMatlab

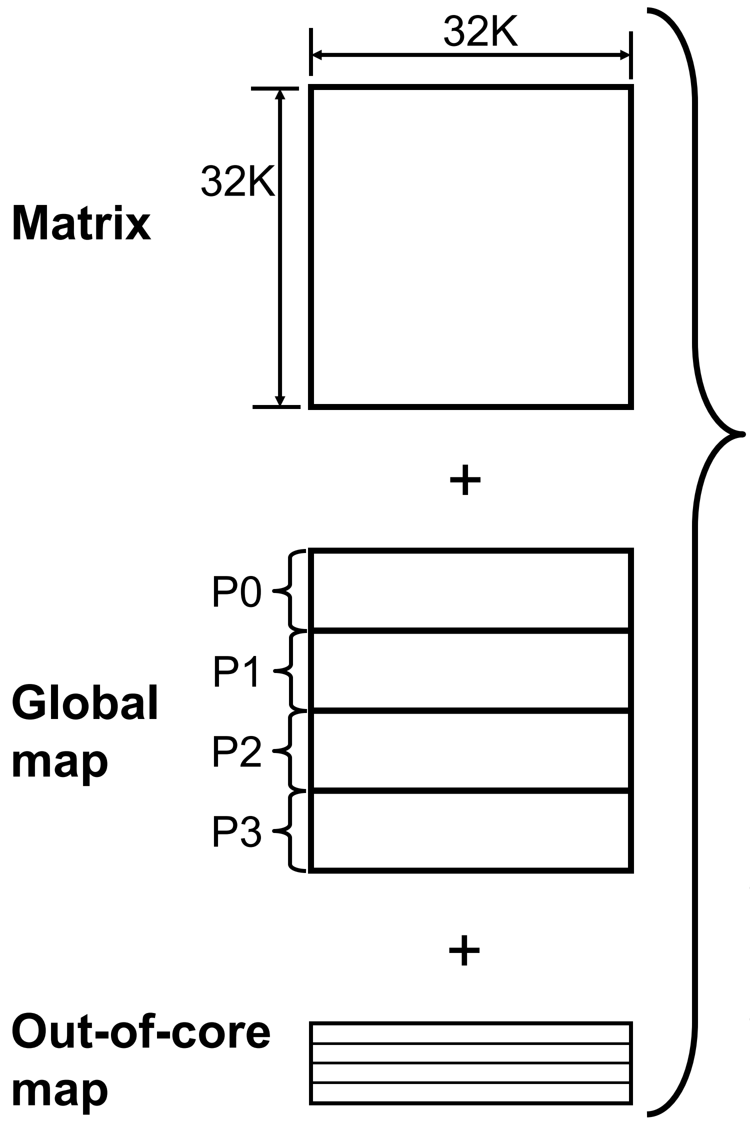
+ Provides mechanism for transparently distributing data across multiple CPUs

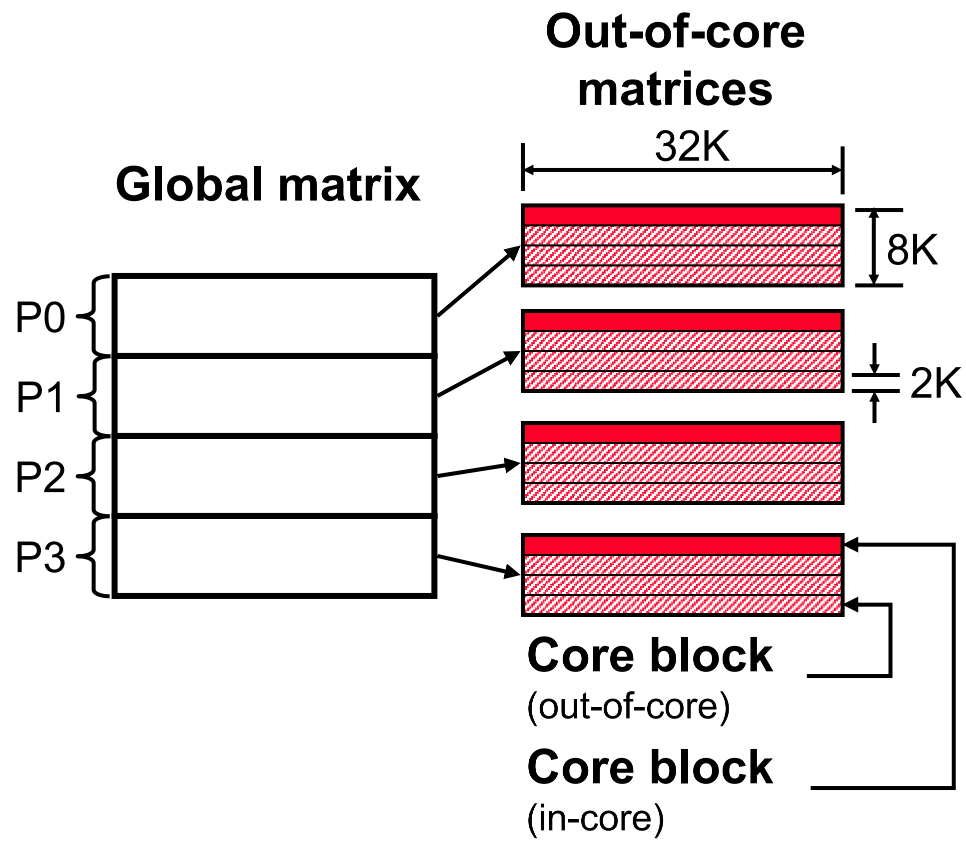
Data Organization

1. **Data starts as a vector with length MN**
2. **Divide into M vectors with length N**
3. **Reorganize as a MxN matrix**
4. **Distribute rows across processors**



Hierarchical Matrices and Maps

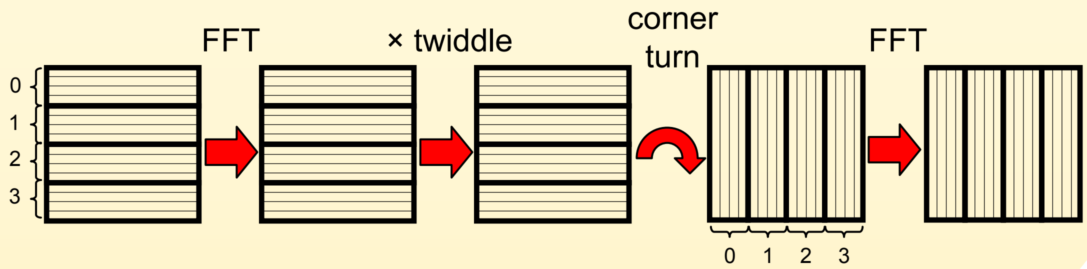




- **Hierarchical matrices span processors and the storage hierarchy**
- **User constructs hierarchy by specifying global and out-of-core maps**

Ultra-long FFT

Ultra-long FFT



Software-based Implementations

MATLAB®

pMatlab C/MPI

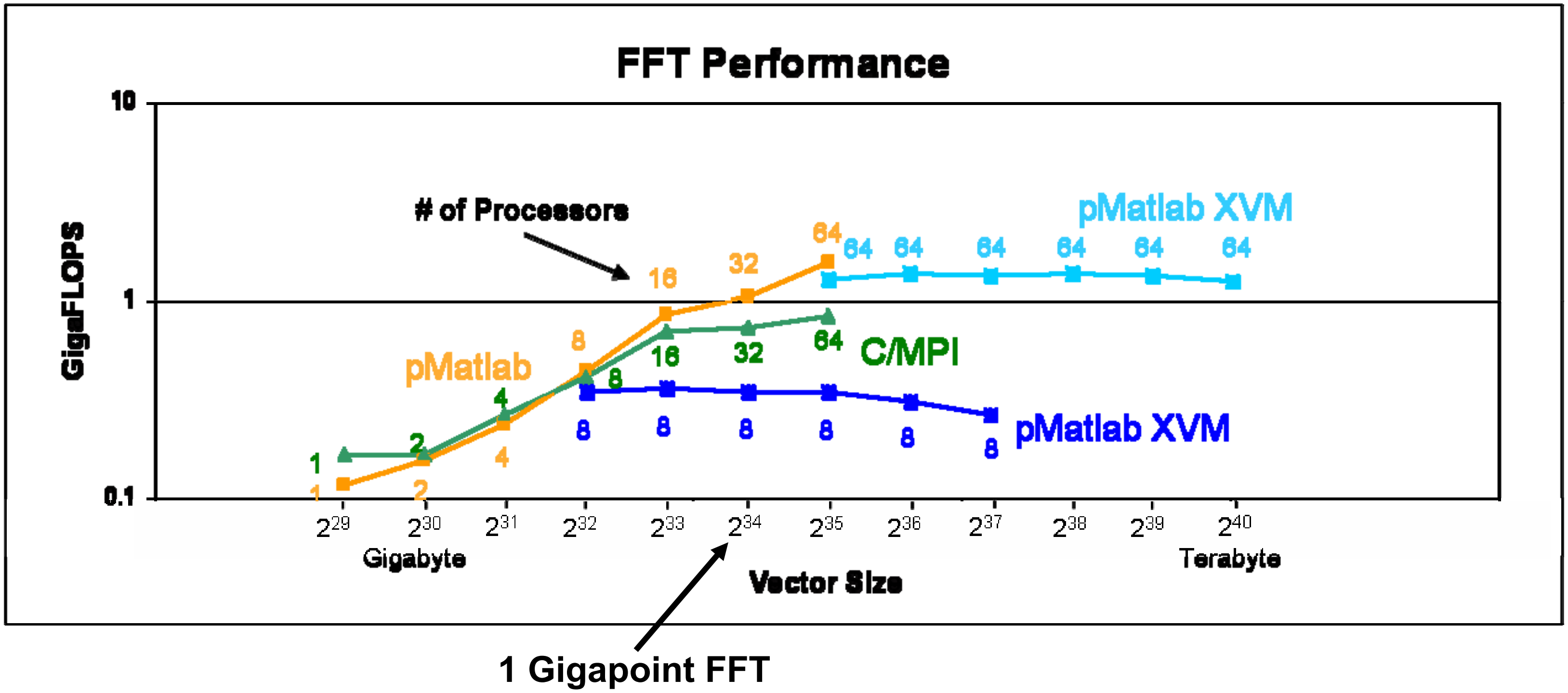
pMatlab XVM

Testbed

Lincoln HPC cluster (LLGrid)

- 80 dual CPU nodes
- 2.8-3.06 GHz Pentium 4 Xeon
- 4 GB memory
- Gigabit Ethernet

Scalability



- pMatlab XVM supports ultra-long FFT's with little degradation in performance
- Maximum problem size = size of available disk space
- 1 TB represents a 64 G-pt double-precision, complex FFT

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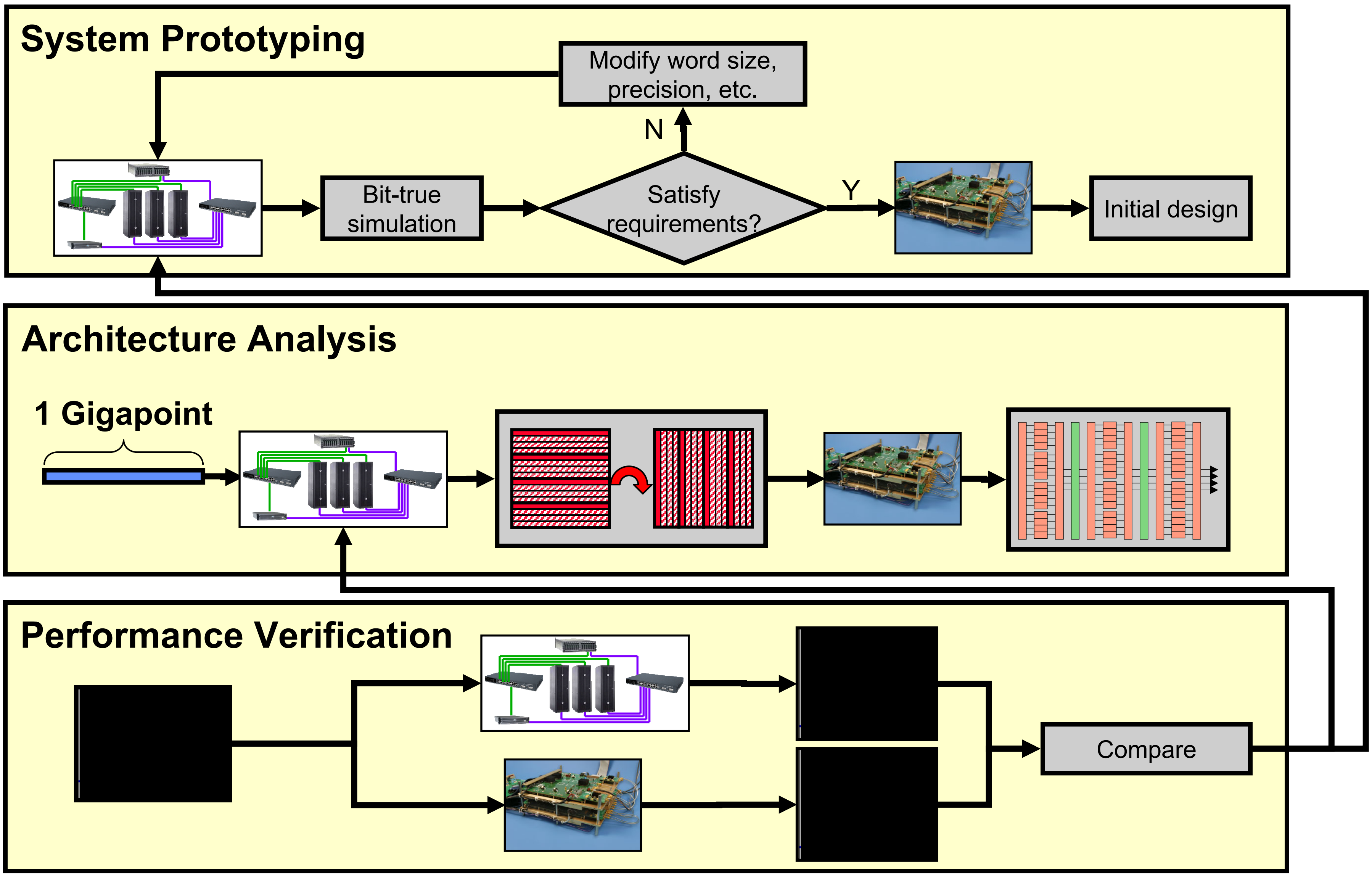
System Development Methodologies



Summary

- Presented FPGA architecture for real-time, ultra-long FFT's
  - Can implement 1 G-pt FFT with smaller FFT's
  - Use SYCO processor to implement FFT's
  - Developed real-time corner turn architecture
- Future
  - Develop a universal ultra-long FFT architecture
  - Allows multiple configurations in same hardware
    - 1 G-Pt FFT
    - 100 M-Pt FFT X 10 channels
  - Application-specific precision and dynamic analysis

Summary

- **Presented parallel software architecture for ultra-long FFT's**
  - **Added out-of-core capability to pMatlab**
  - **Supports ultra-long FFT's with little degradation in performance**
  - **Demonstrated 64 G-pt FFT (1 TB)**
- **Future**
  - **Expand cluster to enable 64 T-pt FFT (1 PB)**

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